

Adaptable Ferroelectric Memories for Space Applications

David A. Kamp, Alan DeVilbiss, Stephen C. Philpy and Gary F. Derbenwick

Abstract

Test results on a 1-kilobit prototype hardened-by-design ferroelectric memory designed by Celis and fabricated by Fujitsu using their commercial ferroelectric process show that the total dose hardness exceeds 2 Mrads and latch-up immunity exceeds 163 LET. Based on the proven prototype memory design concepts, a 2-Mbit hardened by design ferroelectric memory for the JPL JIMO program is being designed. A subsequent design is expected to be at the 32-Mbit density. Using die stacking packaging techniques, components at densities up to 256 Mbits based on this design are being developed. To obtain such high-density products, Celis is collaborating with TI using the TI 0.13-micron commercial ferroelectric process.

Ferroelectric memory is flexible in providing radiation hardened nonvolatile memory for diverse memory systems for space applications. A basic ferroelectric memory core can be combined with on-chip interface circuitry to emulate any number of traditional semiconductor memory architectures, including SRAM, SDRAM, EEPROM and Flash memory. Ferroelectric memory can be used for everything from small boot memories to high-density mass memories. Design rules for ferroelectric memory processes at 0.13 micron and 0.09 micron are competitive with the most aggressive design rules used for other semiconductor memory types. The very fast read and write times, coupled with the ability to trade off internal programming voltage with retention and endurance, enables the ferroelectric memory technology to be so adaptable.

Celis has demonstrated that the inherently radiation hard ferroelectric memory element can be combined with hardened-by-design CMOS and memory array circuitry to provide very high levels of radiation tolerance, without the need for shielding. Because the chips are fabricated on commercial production lines with no special processing for radiation hardness, ferroelectric designs are portable between wafer fabrication facilities.

Description of various architectures and operation modes of ferroelectric memories will be presented. The basic memory core designed for radiation tolerance will be described. Various operating modes of the memory core for each architecture will be presented along with the appropriate interface circuitry.

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Celis Semiconductor Corporation
5475 Mark Dabling Boulevard, Suite 102
Colorado Springs, CO 80918
Phone: (719) 260-9133 Fax: (719) 593-8540
celis@celis-semi.com